ELECTRONIC DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority and benefits of Korean Patent Application No. 10-2014-0182704, entitled "ELECTRONIC DEVICE AND METHOD FOR FABRICATING THE SAME" and filed on Dec. 17, 2014, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] This patent document relates to a memory circuit or a memory device and an electronic device employing the same.

BACKGROUND

[0003] Recently, as electronic appliances trend toward miniaturization, low power consumption, high performance, multi-functionality, and so on, semiconductor devices capable of storing information in various electronic appliances such as a computer, a portable communication device, and so on have been demanded in the art, and research has been conducted for the semiconductor devices. Such semiconductor devices include semiconductor devices which can store data using a characteristic that they are switched between different resistant states according to an applied voltage or current, for example, an RRAM (resistive random access memory), a PRAM (phase change random access memory), an FRAM (ferroelectric random access memory), an MRAM (magnetic random access memory), an E-fuse, etc.

SUMMARY

[0004] The disclosed technology in this patent document provides an electronic device with improved variable resistance characteristics and a method for fabricating the same.

[0005] The disclosed technology in this patent document includes memory circuits or devices and their applications in electronic devices or systems and various implementations of an electronic device in which an electronic device capable of improving the characteristics of a variable resistance element is provided.

[0006] In an aspect, a method for forming an electronic device with a semiconductor memory is provided to include forming a crystalized doped layer over a substrate; forming a barrier layer over the crystalized doped layer; forming a metal layer over the barrier layer; and reacting the barrier layer with a portion of the metal layer.

[0007] Implementations of the above method for forming an electronic device with a semiconductor memory may include one or more the following.

[0008] The forming of the crystalized doped layer includes: doping impurities into the substrate to form a doped region in the substrate; and performing laser annealing to recrystallize the doped region to form the crystalized doped layer. The forming of the barrier layer includes transforming the material structure of a portion of the crystalized doped layer into an amorphous layer. The forming of the barrier layer includes performing ion implantation into the crystalized doped layer. The barrier layer has a depth smaller than the depth of the doped region. The metal layer includes a single layer or a multi-layer. The metal layer includes a stack including a titanium layer and a titanium nitride layer. The reacting of the barrier layer and the portion of the metal layer includes performing heat treatment on the barrier layer and the portion of the metal layer. The reacting of the barrier layer with the portion of the metal layer including forming a silicide layer.

[0009] In another aspect, a method for forming an electronic device with a semiconductor memory is provided to includes forming buried gates in a substrate; forming a recess in the substrate between neighboring buried gates; forming a crystalized doped layer to fill in a lower portion of the recess; forming a landing plug in the recess over the crystalized doped layer, wherein the landing plug includes a stack of a silicide layer and a metal layer; forming an interlayer insulating layer over the substrate including the landing plug; forming a lower electrode contact that passes through the interlayer insulating layer and is in contact with the landing plug; and forming a variable resistance element which is disposed over the interlayer insulating layer and is coupled to the lower electrode contact.

[0010] Implementations of the above method for forming an electronic device with a semiconductor memory may include one or more the following.

[0011] The forming of the crystalized doped layer includes: doping impurities into the substrate under the recess to form a doped region; and performing laser annealing to recrystallize the doped region to form the crystalized doped layer. The forming of the landing plug includes: changing the material structure of the crystalized doped layer to form a barrier layer over the crystalized doped layer; forming the metal layer over the barrier layer to fill the recess; and reacting the barrier layer and a portion of the metal layer. The changing of the material structure of the crystalized doped layer includes transforming a portion of the crystalized doped layer into an amorphous layer. The changing of the material structure of the crystalized doped layer includes performing ion implantation into the crystalized doped layer. The metal layer includes a single layer or a multi-layer. The metal layer includes a stack including a titanium layer and a titanium nitride layer. The reacting of the barrier layer and the portion of the metal layer includes performing heat treatment on the barrier layer and the portion of the metal layer.

[0012] In another aspect, an electronic device is provided to include a semiconductor memory that includes buried gates formed in a substrate; a recess disposed in the substrate between neighboring buried gates; a crystalized doped layer formed in the substrate to fill in a lower portion of the recess; a landing plug formed in the recess over the crystalized doped layer and including a stack that includes a silicide layer and a metal layer; an interlayer insulating layer formed over the substrate including the landing plug; a lower electrode contact passing through the interlayer insulating layer and being in contact with the landing plug; and a variable resistance element formed over the interlayer insulating layer and being in contact with the lower electrode contact.

[0013] Implementations of the above electronic device may include one or more the following.

[0014] The silicide layer includes a titanium silicide layer. The metal layer includes a titanium nitride layer. The variable resistance element includes transitional metal oxide, metal oxide including perovskite material, phase-changing material including chalcogenide material, ferro-